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APPLICATION FOR LETTERS PATENT

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METHODS OF FORMING AN ISOLATION
TRENCH IN A SEMICONDUCTOR, METHODS
OF FORMING AN ISOLATION TRENCH IN A
SURFACE OF A SILICON WAFER, METHODS
OF FORMING AN ISOLATION TRENCH-
ISOLATED TRANSISTOR, TRENCH-ISOLATED
TRANSISTOR, TRENCH ISOLATION
STRUCTURES FORMED IN A SEMICONDUCTOR,
MEMORY CELLS AND DRAMS

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1 METHODS OF FORMING AN ISOLATION TRENCH IN A
2 SEMICONDUCTOR, METHODS OF FORMING AN ISOLATION
3 TRENCH IN A SURFACE OF A SILICON WAFER, METHODS OF
4 FORMING AN ISOLATION TRENCH-ISOLATED TRANSISTOR,
5 TRENCH-ISOLATED TRANSISTOR, TRENCH ISOLATION
6 STRUCTURES FORMED IN A SEMICONDUCTOR, MEMORY CELLS
7 AND DRAMS

8 TECHNICAL FIELD

9 The present invention relates to methods of forming an isolation
10 trench in a semiconductor, methods of forming an isolation trench in a
11 surface of a silicon wafer, methods of forming an isolation trench-isolated
12 transistor, trench-isolated transistor, trench isolation structures formed in
13 a semiconductor, memory cells and DRAMs.

14 BACKGROUND OF THE INVENTION

15 Field-effect transistors ("FETs") are used in memory structures such
16 as dynamic random access memories ("DRAMs") for controlling access
17 to capacitors used to store charge representing information contained in
18 the memories. In DRAMs, charge leakage effects necessitate periodic
19 refreshing of the information stored in the memory. In turn, refreshing
20 of the DRAM leads to increased power consumption and delays in
21 memory operation. Accordingly, it is desirable to reduce charge leakage
22 effects in DRAMs.

23 Additionally, it is desirable to minimize the area required for
fabrication of the elements of memories such as DRAMs. Electrical
isolation of various circuit elements from each other is required. In

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1 turn, electrical isolation requires some of the space used on the DRAM
2 or other integrated circuitry. Various techniques have been developed
3 to reduce the amount of area needed for electrical isolation structures.
4 One technique for providing a high degree of electrical isolation while
5 requiring relatively little space is known as shallow trench isolation.

6 One source of charge leakage in DRAMs is related to carrier
7 generation-recombination phenomena. In general, lower dopant
8 concentrations tend to reduce this source of charge leakage. However,
9 other concerns tend to determine lower bounds for dopant concentrations.

10 The FETs used as access transistors determine some of these other
11 concerns. The FETs need to be able to provide a high impedance when
12 they are turned OFF, and a low impedance connection when they are
13 turned ON. DRAMs and other memories use an addressing scheme
14 whereby a wordline that is coupled to many transistor gates is selected,
15 and at the same time a bitline or digitline that is coupled to many
16 transistor drains is also selected. A FET that is located at the
17 intersection of the selected wordline and the selected bitline is turned
18 ON, and that memory cell is accessed. At the same time, many other
19 FETs have a drain voltage due to the drains of these FETs being
20 coupled to the selected bitline. These FETs exhibit some parasitic
21 conductance as a result of the drain voltage. In some types of
22 integrated circuits, a portion of that parasitic conductance is due to
23 corner effects that are an artifact of using Trench isolation techniques

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1 to isolate the FETs from one another and from other circuit elements.

2 These effects are described in "Subbreakdown Drain Leakage
3 Current in MOSFET" by J. Chen et al., IEEE El. Dev. Lett., Vol.
4 EDL-8, No. 11, Nov. 1987; "Impact Of Shallow Trench Isolation On
5 Reliability Of Buried- And Surface-Channel Sub- μ m PFET" by W. Tonti
6 and R. Bolam, IEEE Cat. No. 0-7803-2031, 1995; "Shallow Trench
7 Isolation For Advanced ULSI CMOS Technologies", M. Nandakumar et
8 al.; and "Shallow Trench Isolation Characteristics With High-Density-
9 Plasma Chemical Vapor Deposition Gap-Fill Oxide For Deep-Submicron
10 CMOS Technologies", S.-H. Lee et al., Jpn. J. Appl. Phys.,
11 Vol. 37, 1998, pp. 1222-1227, which publications are hereby incorporated
12 herein by reference for their general background teachings.

13 One method of reducing these parasitic conduction effects is to
14 round the corner where the isolation trench meets the surface of the
15 semiconductor material. This may be effected by oxidizing the surface
16 of the silicon, as is described in the above-noted publications. However,
17 this approach requires additional processing steps, which tend to result
18 in reduced yield, among other things.

19 What is needed is a way to incorporate trench isolation together
20 with FETs that does not increase processing complexity and that provides
21 compact, low-leakage transistors in DRAMs and other circuitry.

1 SUMMARY OF THE INVENTION

2 In one aspect, the present invention provides a method of forming
3 an isolation trench in a semiconductor. The method includes forming
4 a first isolation trench portion having a first depth and having a first
5 sidewall intersecting a surface of the semiconductor at a first angle. The
6 method also includes forming a second isolation trench portion within
7 and extending below the first isolation trench portion. The second
8 isolation trench portion has a second depth and includes a second
9 sidewall. The second sidewall intersects the first sidewall at an angle
10 with respect to the surface that is greater than the first angle. A
11 dielectric material fills the first and second isolation trench portions.

12 In another aspect, the present invention includes a method of
13 forming an isolation trench in a surface of a silicon wafer. The method
14 includes forming a mask on the surface, where the mask includes an
15 opening and sidewalls, and etching the silicon surface using gases
16 including CF_4 and CHF_3 in a ratio of $\text{CF}_4/\text{CHF}_3 = 0.11$ to 0.67 to form
17 a first isolation trench portion.

18 In a further aspect, the present invention includes a trench-isolated
19 transistor. The trench-isolated transistor includes first and second
20 isolation trenches each disposed on a respective side of a portion of
21 silicon. The first and second isolation trenches each include a first
22 isolation trench portion having a first depth and having a first sidewall
23 intersecting a surface of the silicon at a first angle. The first and

1 second isolation trenches each also include a second isolation trench
2 portion within and extending below the first isolation trench portion.
3 The second isolation trench portion has a second depth and includes a
4 second sidewall intersecting the first sidewall at an angle with respect to
5 the surface that is greater than the first angle. The first and second
6 isolation trenches are filled with a dielectric material. The transistor
7 further includes a gate extending across the silicon portion from the first
8 isolation trench to the second isolation trench, and source and drain
9 regions extending between the first and second isolation trench portions
10 and across the silicon portion. The source region is adjacent one side
11 of the gate and the drain region is adjacent another side of the gate
12 that is opposed to the one side.

13 14 BRIEF DESCRIPTION OF THE DRAWINGS

15 Preferred embodiments of the invention are described below with
16 reference to the following accompanying drawings.

17 Fig. 1 is a simplified plan view of shallow trench isolation
18 structures and a FET, in accordance with an embodiment of the present
19 invention.

20 Fig. 2 is a simplified side view, in section, taken along section
21 lines 2-2 of Fig. 1, of the shallow trench isolation structures and FET
22 of Fig. 1, in accordance with an embodiment of the present invention.
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Fig. 3 is a simplified side view, in section, illustrating formation of a trench isolation structure, in accordance with an embodiment of the present invention.

Fig. 4 is a simplified flow chart of a process for forming the structures of Figs. 1 and 2, in accordance with an embodiment of the present invention.

Fig. 5 is a simplified schematic diagram of a memory cell that advantageously employs the structures of Figs. 1 and 2, in accordance with an embodiment of the present invention.

Fig. 6 is a simplified block diagram of a DRAM that advantageously employs the structures of Figs. 1, 2 and 5, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the Progress of Science and useful Arts" (Article 1, Section 8).

Fig. 1 shows trench isolation structures 10 and a FET 12 formed in a semiconductor substrate 13, in accordance with but one preferred embodiment of the present invention. The FET 12 includes a gate G, which may be formed from polysilicon, a source S and a drain D. The trench isolation structures 10 each include a first isolation trench portion 14 having a first depth 16 and having first sidewalls 18 each

1 intersecting a surface 20 of the semiconductor substrate 13 at a first
2 angle θ_1 .

3 The trench isolation structures 10 also each include a second
4 isolation trench portion 24 within and extending below the first isolation
5 trench portion 14. The second isolation trench portions 24 have a
6 second depth 26 and include second sidewalls 28 each intersecting one
7 of the first sidewalls 18 at a second angle θ_2 with respect to the
8 surface 20 that is greater than the first angle θ_1 to form shoulders 30
9 at the juncture of the first sidewall 18 and the second sidewall 28.

10 In one embodiment, the shoulders 30 result in substantial reduction
11 of subthreshold current through the FET 12. In other words, when the
12 FET 12 is OFF, the amount of current that can be induced in the
13 FET 12 by applying voltage to the drain D is greatly reduced.

14 In one embodiment, the first angle θ_1 is less than about sixty
15 degrees and the second angle θ_2 is eighty degrees or more. In one
16 embodiment, the first angle θ_1 is in a range of from about five degrees
17 to about forty-five degrees. In one embodiment, the first angle θ_1 is in
18 about thirty-five degrees. In one embodiment, the first angle θ_1 is about
19 forty degrees. The concerns addressed in selecting the first angle θ_1 are
20 to select an angle θ_1 providing a shoulder that reduces electrical fields
21 in the subsequently-formed FET 12 and to also select an angle that does
22 not impede subsequent filling of the trench isolation structures 10 with
23 dielectric material such as silicon dioxide.

1 Further in the illustrated embodiments, substantially straight linear
2 segment 18 extends entirely between and to outermost surface portion 20,
3 respectively, and to segment 28. Substantially straight linear segment 28
4 extends from segment 18 to a bottom of the trench isolation
5 structure 10.

6 Alternate embodiments are, of course, contemplated whereby some
7 substantially straight linear segment occurs somewhere within each of first
8 sidewalls 18 and second sidewalls 28, without extending over the entirety
9 of the first 18 and second 28 sidewalls. In the context of this patent,
10 "substantially straight linear" means a perfectly straight segment as well
11 as a segment that has a degree of curvature associated with it. A
12 curved segment is to be considered "substantially straight linear" in the
13 context of this patent provided that it has some chord length greater
14 than or equal to 30 nanometers and has some radius of curvature of at
15 least 20 nanometers.

16 The first sidewall 18 needs to incorporate a lateral dimension wide
17 enough such that wet dips occurring during processing steps such as
18 nitride hard mask removal and those subsequent up to gate oxide growth
19 do not start to etch down the sidewall of the isolation trench
20 structure 10. That dimension is proportional to the various dielectric
21 layer thicknesses, and so can vary greatly from process to process and
22 through different technology generations. Exemplary minimum extents for
23

1 the first sidewalls 18, i.e., distance from the top surface 20 to the
2 shoulder 30, are in a range of from 50 Angstroms to 500 Angstroms.

3 Fig. 3 is a simplified side view, in section, illustrating formation
4 of a trench isolation structure, in accordance with an embodiment of the
5 present invention. In one embodiment, the trench isolation structures 10
6 are created by forming a masking layer 32 on the semiconductor
7 surface 20. In one embodiment, the masking layer 32 includes a silicon
8 dioxide layer 34 having a thickness of about 100 Angstroms and a silicon
9 nitride layer 36 having a thickness of about 1000 Angstroms. A
10 photoresist layer 38 is formed on the masking layer 32, and openings 40
11 corresponding to the trench isolation structures 10 are formed in the
12 photoresist. The openings 40 have sidewalls 42.

13 In one embodiment, a plasma etch is used to form openings in the
14 masking layer 32. The plasma etch is also used to etch the first isolation
15 trench portions 14. In one embodiment, the plasma etch is performed
16 using a mixture of fluorocarbon and fluorohydrocarbon gases, such as, by
17 way of example, CF_4 , CHF_3 , CH_2F_2 and/or C_2F_8 or the like. In one
18 embodiment, the plasma etch is performed using a mixture of CF_4 and
19 CHF_3 in a ratio ranging from 0.11 to 0.67.

20 In one embodiment, the masking layer 32 is etched, and then
21 etching is continued for a predetermined time to etch the first isolation
22 trench portion 14. In one embodiment, the etching is carried out for 30
23 seconds, where the first half of the etching process is used to broach

the masking layer 32. In one embodiment, the etching is carried out for 40 seconds. A broad variety of implementations are possible, using different etch gas compositions, pressures and etch times, as may be seen by comparing these examples to the example below. In one embodiment, etching is carried out using parameters given below in Table I in a Hitachi microwave etcher model 511A, using the photoresist 38, silicon nitride 36 and silicon dioxide 34 mask structure 32 described above.

TABLE I

EXEMPLARY SHOULDER FORMATION PROCESSING PARAMETERS

Parameter	Units	Mask etch	Overetch	Trench	De-chuck
Step time	seconds	60	22	78	1.0
Gas 1	sccm	200	200	0	150
Gas 2	sccm	160	60	0	0
Gas 3	sccm	40	140	0	0
Gas 4	sccm	0	0	100	0
Gas 5	sccm	0	0	5.7	0
Pressure	mTorr	20	20	6	7.5
Power 1	W	550	550	800	1000
Power 2	W	90	130	60	0

Notes: gas 1 corresponds to argon, gas 2 corresponds to CF₄, gas 3 corresponds to CHF₃, gas 4 corresponds to HBr, gas 5 corresponds to O₂, power 1 corresponds to magnetron power and power 2 corresponds to applied RF power.

The shoulder 30 is formed by a process whereby a polymer 44 is formed on the sidewalls 42. By adjusting the composition of the etching gases, applied RF power, chamber pressure and the like, the polymer 44 is formed at a rate that encourages a particular first angle θ_1 to be formed during the etching process. By stopping the etching and polymer deposition at the end of the predetermined time interval, the first

1 depth 16 can be controlled. The second isolation trench portion 24 is
2 then etched, using a different etch gas mixture, for example, as noted
3 in Table I.

4 In another embodiment, a first etch is carried out to provide the
5 first isolation trench portion 14. A second masking step is then carried
6 out, and openings corresponding to the second isolation trench
7 portion 24 are created. The second isolation trench portion 24 is then
8 etched.

9 In one embodiment, the first depth 16 is chosen to be five to
10 thirty or fifty percent of the total trench depth, i.e., the first depth 16
11 plus the second depth 26. In one embodiment, the first depth 16 is
12 chosen to be five to fifteen percent of the total trench depth. In one
13 embodiment, bottoms of the trenches are implanted with dopant after the
14 first 14 and second 24 trench portions are etched. This allows a
15 shallower trench to be employed, and results in the first depth 16 being
16 a larger percentage of the total trench depth.

17 In one embodiment, implant doses required to form the source S
18 and drain D regions are reduced by as much as ten percent when the
19 shoulder 30 is present, resulting in an increase of as much as thirty
20 percent of the time required between refresh cycles. For example, if a
21 typical implant dose of $5.4 \times 10^{12}/\text{cm}^2$ were ordinarily required to dope
22 channel regions, a dose of $4.9 \times 10^{12}/\text{cm}^2$ could be employed together with
23 formation of the shoulder 30.

Following etching of the first 14 and second 24 isolation trench portions, the photoresist layer 38 and the polymer 44 may be stripped using a conventional oxygen ashing process. A dielectric material, typically silicon dioxide, may be used to fill the first 14 and second 24 isolation trench portions, and conventional chemical-mechanical polishing may be used to planarize the resultant structure. In one embodiment, plasma etchback is employed to planarize the dielectric material, usually together with another patterning step or a planarizing coating layer. The gate G may be formed using conventional polysilicon, polycide or metal, and the source S and drain D may be formed using conventional ion implantation techniques or doping outdiffusion from subsequent layers.

Fig. 4 is a simplified flow chart of a process P1 for forming the structures of Figs. 1 and 2, in accordance with an embodiment of the present invention.

In a step S1, the first isolation trench portions 14 are formed. In one embodiment, the first isolation trench portions 14 are formed by forming the masking layer 32, followed by plasma etching, as described above.

In a step S2, the second isolation trench portions 24 are formed. In one embodiment, the second isolation trench portions 24 are formed by etching as described above with reference to Fig. 3 and Table I. In one embodiment, the second isolation trench portions 24 are formed by separate masking and etching operations.

1 In a step S3, the first 14 and second 24 trench portions are filled
2 with a dielectric using conventional processing techniques as described
3 above. The step S3 may include planarization of the dielectric material,
4 for example via conventional chemical-mechanical polishing.

5 In a step S4, the FET 12 is formed, using conventional processing
6 techniques, as discussed above. The process P1 then ends, and
7 processing continues using conventional processing operations.

8 Fig. 5 is a simplified schematic diagram of a memory cell 50 that
9 advantageously employs the structures of Figs. 1 and 2, in accordance
10 with an embodiment of the present invention. The memory cell 50
11 includes the FET 12 of Figs. 1 and 2, a capacitor 52 coupled to the
12 source S of the FET 12, a wordline 54 coupled to the gate G (and to
13 other gates in other memory cells) and a bitline 56 coupled to the
14 drain D of the FET 12 (and to other drains in other memory cells).
15 By selecting the wordline 54 and the bitline 56, the FET 12 is turned
16 ON, and charge stored in the capacitor 52 can then be measured to
17 determine the datum stored in the memory cell 50. Alternatively, by
18 selecting and turning the FET 12 ON, charge can be injected into the
19 capacitor 52 to write a datum therein, and the FET 12 can then be
20 turned OFF to store the datum in the memory cell 50.

21 Fig. 6 is a simplified block diagram of a DRAM 60 that
22 advantageously employs the structures of Figs. 1, 2 and 5, in accordance
23 with an embodiment of the present invention. The DRAM 60 includes

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1 a memory cell array 62 coupled to a group of wordlines 56 and a group
2 of bitlines 54. Address decoders, such as a row decoder 64 and a
3 column decoder 68, decode addresses provided via a bus, allowing data
4 to be read from or written to memory cells 50 in the memory cell
5 array 62.

6 In compliance with the statute, the invention has been described
7 in language more or less specific as to structural and methodical
8 features. It is to be understood, however, that the invention is not
9 limited to the specific features shown and described, since the means
10 herein disclosed comprise preferred forms of putting the invention into
11 effect. The invention is, therefore, claimed in any of its forms or
12 modifications within the proper scope of the appended claims
13 appropriately interpreted in accordance with the doctrine of equivalents.
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